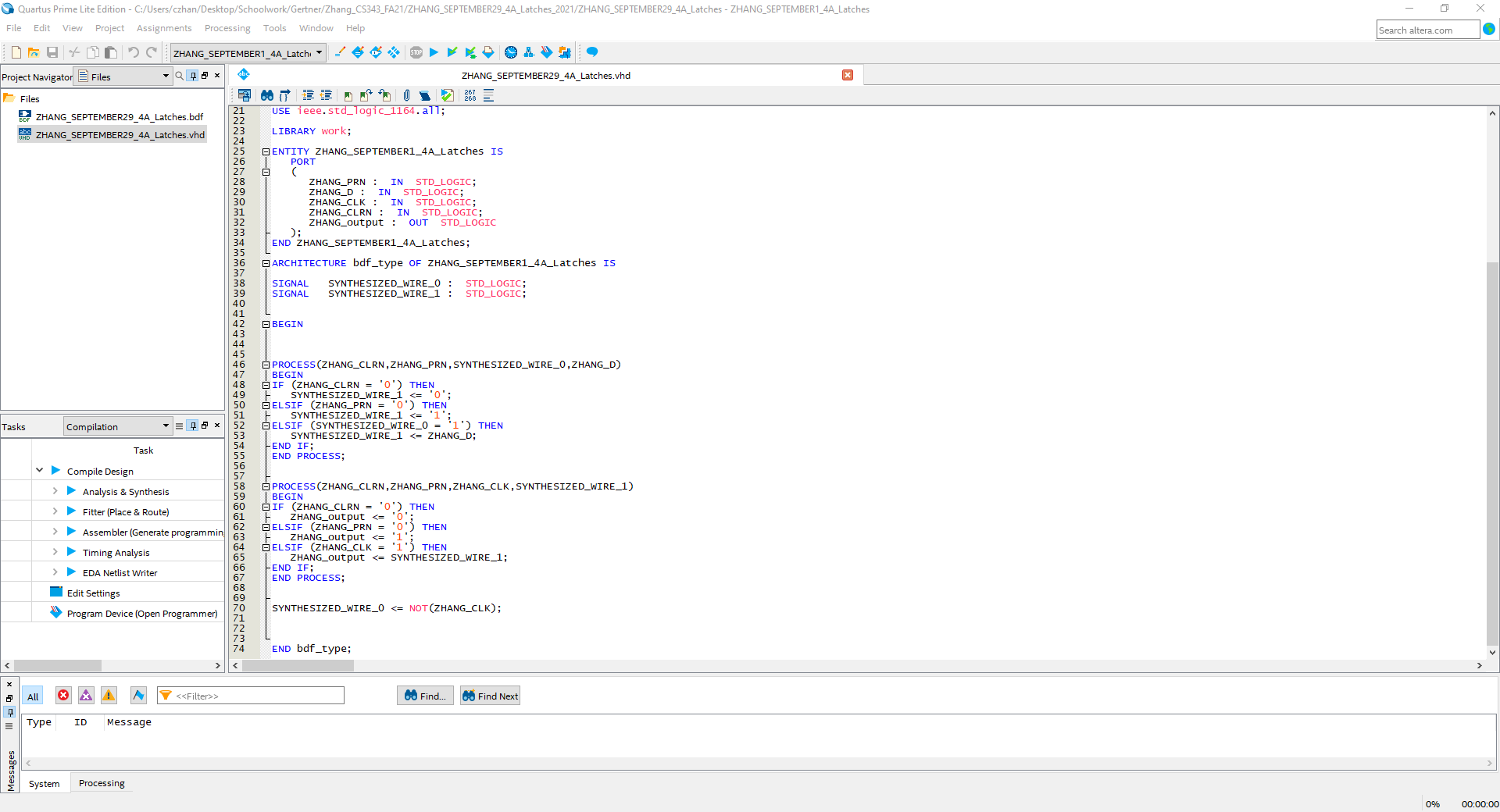
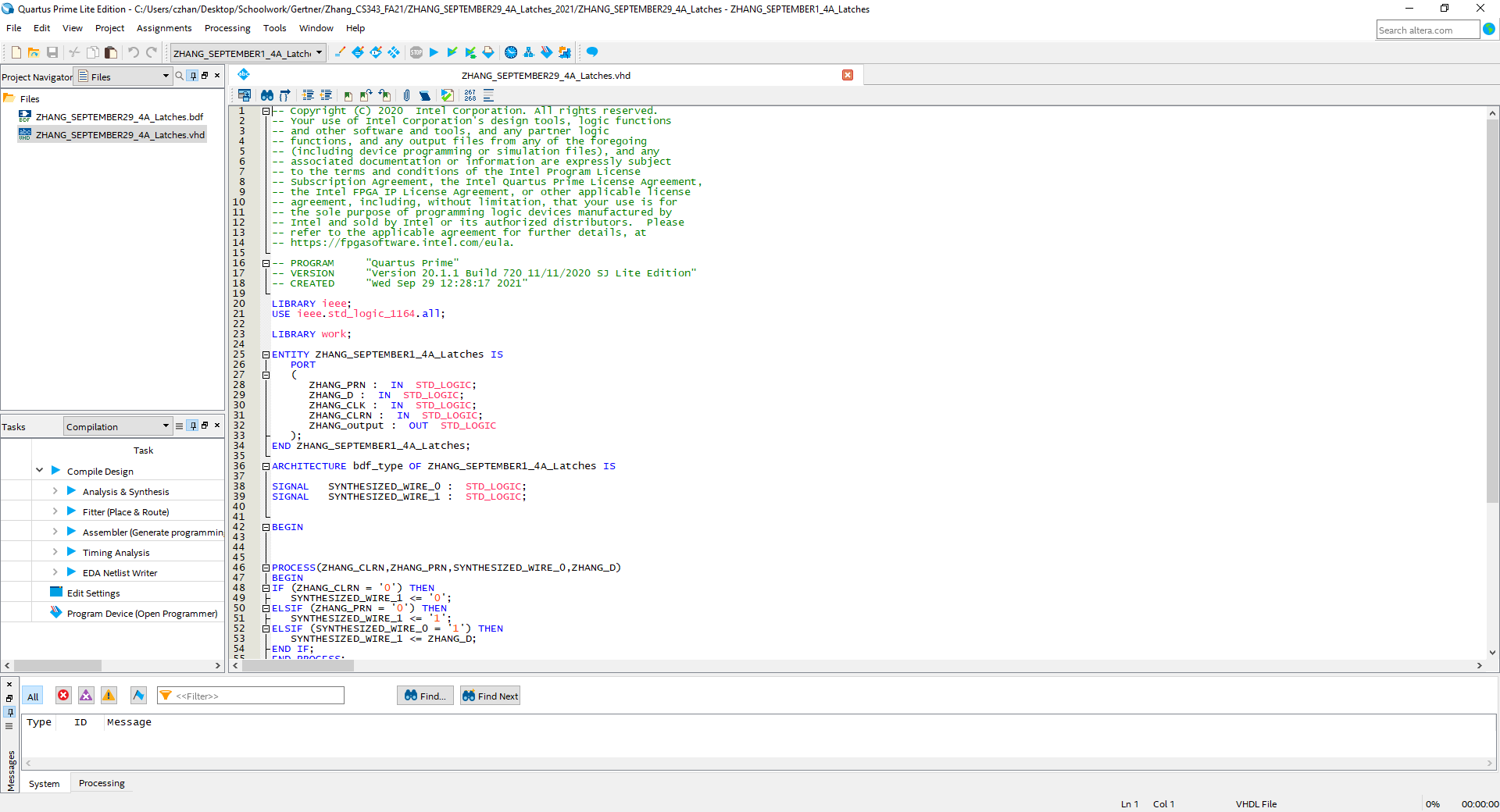
Review Lab : Master Slave

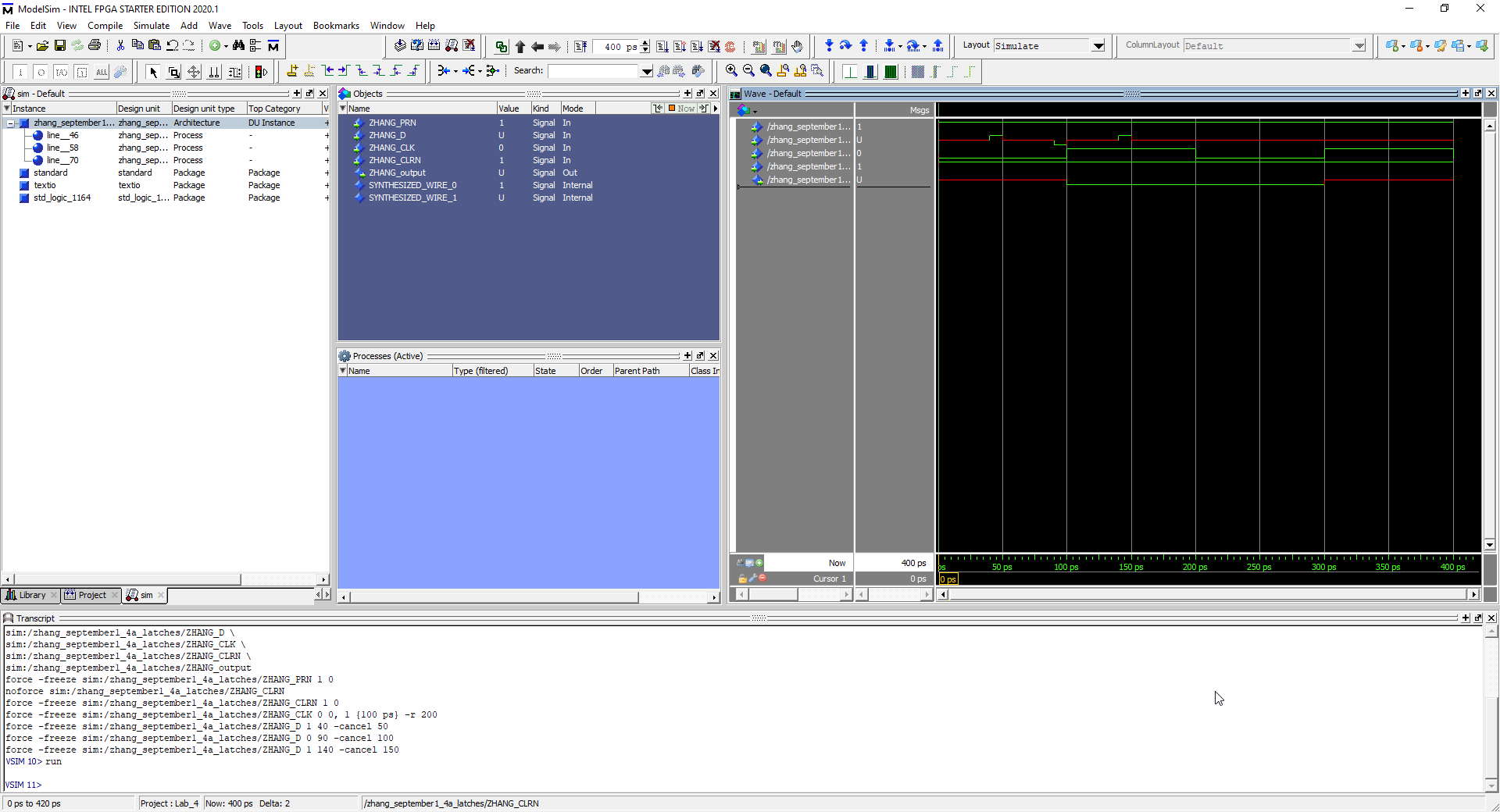
Chue Zhang

Csc343 Fall 2021

Professor Gertner



Lpm generated D latches which were used to create a master slave flip flop design.



Clock is at 200ps intervals with input data D at 40ps-50ps, 90ps-100ps, 140ps-150ps. First input nothing because not positive edge triggered, second input is positive edge triggered so you notice output result and third input is no changes.